regions for forming a plurality of functional blocks;

a region for forming wiring layers for connecting the functional blocks,

wherein each of the regions for forming the functional blocks includes a multilayer wiring, and

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wherein the region for forming the wiring layers for connecting the functional blocks includes wiring layers thicker than those in the functional blocks, and a bottom surface of a wiring layer in the multilayer wiring provided in the region for forming the functional block is on the same plane as a bottom surface of the wiring layer provided in the region for forming the wiring layers for connecting the functional blocks as viewed cross sectionally.

REMARKS

This is in response to the Office Action dated August 14, 2002. Non-elected claims 6-9 have been canceled, without prejudice in view of the Restriction Requirement. Claims 1-5 are now pending. Attached hereto is a marked-up version of the changes made to the specification and claim(s) by the current amendment. The attached page(s) is captioned "**Version With Markings To Show Changes Made.**"

The specification stands objected to in paragraph 2 of the Office Action. It is respectfully submitted that the specification amendment herein addresses and overcomes any potential issue in this respect.

The claims stand objected to in paragraph 3 of the Office Action. It is respectfully submitted that the claim changes herein address and overcome any potential issue in this regard.

For purposes of example, and without limitation, certain example embodiments of this invention relate to a wiring structure for conductively connecting adjacent functional blocks in a semiconductor device. Fig. 2 of the instant application illustrates a plurality of adjacent functional blocks 7 to be connected via wiring structure in region 8. Fig. 3(1) is a cross sectional view of an example functional block 7 from Fig. 2. Meanwhile, *Figs. 3(2) and 3(3)* are *cross sectional views* illustrating wiring structure in region 8 for *connecting* adjacent blocks 7 according to first and second different embodiments of this invention. In the Fig. 3(2) embodiment, the wiring structure in connection region 8 comprises a *coaxial line* that includes an *inner* signal line 17 and an *outer* ground line 12, 15, 16, 20, 21. The term "coaxial" means that the inner and outer lines have a common axis along a longitudinal extent of at least part of the line. It can be seen that an insulator 19 is provided between the inner and outer lines in Fig. 3(2). In the Fig. 3(3) embodiment, the wiring structure in connection region 8 comprises a transmission line including a central signal line 18 sandwiched between lower and upper ground or power lines 12, 21. Again, when viewed cross sectionally in Fig. 3(3), it can be seen that an insulator 19, 14 is provided between central signal line 18, and the upper/lower lines 12, 21. Example advantages associated with certain embodiments of the instant invention are discussed at page 24, lines 13-20. Another example embodiment is shown cross sectionally in Fig. 11(B-5); in this embodiment wiring 65 in the region for forming the

wiring layers for connecting the functional blocks includes wiring layers 65 *thicker* than those in the functional blocks shown in Fig. 11(A-5).

It is noted that independent claim 1 is directed toward the Fig. 3(2) embodiment; independent claim 3 is directed toward the Fig. 3(3) embodiment, and independent claim 5 is directed toward the Fig. 11 (B-5) embodiment.

Claim 1 stands rejected under 35 U.S.C. Section 103(a) as being allegedly unpatentable over Aoki in view of Abe. This Section 103(a) rejection is respectfully traversed for at least the following reasons.

Claim 1 requires that "the region for forming the wiring layers for connecting adjacent functional blocks includes a coaxial line comprising an inner signal line and an outer ground line surrounding the signal line via an insulating film as viewed cross sectionally, so that the inner signal line and outer ground line have a common axis along at least a portion of a length of the coaxial line." For example, see Fig. 3(2) of the instant application which illustrates that the region 8 for connecting adjacent functional blocks 7 includes a coaxial line including an inner signal line 17 and an outer ground line 12, 15, 16, 20, 21 surrounding the inner signal line 17 via a white insulating film as viewed cross sectionally. See also Figs. 5(B-2) and 10(B-3). The cited art fails to disclose or suggest the aforesaid quoted aspect of claim 1, whether taken alone or in the alleged combination.

Aoki in Fig. 14 illustrates a *top view* which discloses a pair of ring-shaped power supply wirings 905 for supplying power to a plurality of circuit elements/blocks 903. Fig. 14 of Aoki is similar to Fig. 17 in that it too is a *top view* illustrating a ring-shaped power supply wiring 1205 that supplies power to circuit element/block 1203. The *top*

views of Figs. 14 and 17 of Aoki are entirely unrelated to the invention of claim 1 which describes the claimed wirings as viewed *cross sectionally*. In this regard, Aoki significantly differs from the invention of claim 1 which covers, *inter alia*, the Fig. 3(2) embodiment of the instant invention in that Aoki fails to disclose or suggest a connection portion including a "coaxial line comprising an inner signal line and an outer ground line surrounding the signal line via an insulating film as viewed cross sectionally, so that the inner signal line and outer ground line have a common axis along at least a portion of a length of the coaxial line." Aoki is entirely unrelated to the invention of claim 1 in this regard.

Abe is cited merely for the teaching of a multi-layered wiring. Thus, even if Aoki and Abe were combined as alleged in the Office Action (which applicant believes would be incorrect in any event), the invention of claim 1 still would not be met.

Claim 3 states that "each of the regions for forming the functional blocks includes a multilayer wiring, and the region for forming the wiring layers for connecting the functional blocks includes a transmission line comprising a signal line and ground lines and/or power source lines formed above and below the signal line, respectively, as viewed cross sectionally, to sandwich the signal line via an insulating film." For example, see Fig. 3(3) of the instant application which illustrates a connection portion including a transmission line comprising a signal line 18 and ground and/or power source lines 12, 21 formed above and below the signal line 18, respectively, as viewed cross sectionally, to sandwich the signal line via an insulating film 19, 14. The cited art fails to

disclose or suggest the aforesaid quoted aspect of claim 3, whether taken alone or in the alleged combination.

As explained above, the top views of Figs. 14 and 17 of Aoki are entirely unrelated to the invention of claim 3 which describes the claimed wirings as viewed cross sectionally. In this regard, Aoki significantly differs from the invention of claim 3 which covers, *inter alia*, the Fig. 3(3) embodiment of the instant invention. In particular, Aoki fails to disclose or suggest a connection portion including a "transmission line comprising a signal line and ground lines and/or power source lines formed above and below the signal line, respectively, as viewed cross sectionally, to sandwich the signal line via an insulating film" as required by claim 3. Abe also fails to meet this aspect of claim 3. Thus, even if the two references were combined as alleged in the Office Action (which applicant believes would be incorrect in any event), the invention of claim 3 still would not be met.

Claim 5 requires that "the region for forming the wiring layers for connecting the functional blocks includes wiring layers *thicker* than those in the functional blocks, and a bottom surface of a wiring layer in the multilayer wiring provided in the region for forming the functional block is on the same plane as a bottom surface of the wiring layer provided in the region for forming the wiring layers for connecting the functional blocks as viewed cross sectionally." For example, see Fig. 11(B-5) of the instant application which illustrates a connection portion including wiring layers 65 that are thicker than those in the Fig. 11(A-5) functional block. Again, neither Aoki, Abe, nor Parikh

discloses or suggests this aspect of claim 5. The cited art is entirely unrelated to the invention of claim 5 in this respect.

For at least the foregoing reasons, it is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

The paragraph beginning at page 1, line 4:

This application is related to Japanese application No. 2000-371625 filed on December 6, 2000, whose priority is claimed under 35 USC §119[, the disclosure of which is incorporated by reference in its entirety].

IN THE CLAIMS

Please cancel non-elected claims 6-9, without prejudice in view of the Restriction Requirement.

1. (Amended) A semiconductor device comprising:

regions for forming a plurality of functional blocks; [and]

a region for forming wiring layers for connecting the functional blocks,

wherein each of the regions for forming the functional blocks includes a multilayer wiring, and

wherein the region for forming the wiring layers for connecting adjacent functional blocks includes a coaxial line [comprised of] comprising an inner signal line and an outer ground line surrounding the signal line via an insulating film as viewed cross sectionally, so that the inner signal line and outer ground line have a common axis along at least a portion of a length of the coaxial line.

2. (Amended) A semiconductor device according to claim 1, wherein a bottom surface of [any] a wiring in the multilayer wiring provided in the region for forming the functional block is on the same plane as a bottom surface of the coaxial line provided in the region for forming the wiring layers for connecting the functional blocks.

3. (Amended) A semiconductor device comprising:

regions for forming a plurality of functional blocks; and

a region for forming wiring layers for connecting the functional blocks,

wherein each of the regions for forming the functional blocks includes a multilayer wiring, and the region for forming the wiring layers for connecting the functional blocks includes a transmission line comprising a signal line and ground lines and/or power source lines formed above and below the signal line, respectively, as viewed cross sectionally, to sandwich the signal line via an insulating film.

4. (Amended) A semiconductor device according to claim 3, wherein a bottom surface of [any] a wiring layer in the multilayer wiring provided in the region for forming the functional block is on the same plane as a bottom surface of the ground line or power source line located below the transmission line provided in the region for forming the wiring layers for connecting the functional blocks.

5. (Amended) A semiconductor device comprising:

regions for forming a plurality of functional blocks; [and]

a region for forming wiring layers for connecting the functional blocks,

wherein each of the regions for forming the functional blocks includes a multilayer wiring, and

wherein the region for forming the wiring layers for connecting the functional blocks includes wiring layers thicker than those in the functional blocks, and a bottom surface of [any] a wiring layer in the multilayer wiring provided in the region for forming the functional block is on the same plane as a bottom surface of the wiring layer provided in the region for forming the wiring layers for connecting the functional blocks as viewed cross sectionally.